

REMARKS

This Amendment is responsive to the final Office Action dated September 17, 2004. In this Amendment, Applicant has amended claims 1, 16, 21, and 28. Claims 1-4, 6-29, 31 and 32 are pending in the present application.

Applicant respectfully requests entry of this Amendment. The amendments to claims 1, 21, and 28 were not presented earlier in light of the amendments already made to those claims in the previous Amendment dated August 3, 2004. The new amendments to claims 1, 21, and 28 are now presented in response to the latest remarks provided by the Examiner in the final Office Action, in an effort to place the application in condition for immediate allowance. The new amendments should present no new issues, nor require any further search.

Allowable Subject Matter

In the final Office Action, the Examiner allowed claims 9, 10, 16, 20, 25, 26 and 32.

Amendments

Applicant has amended claims 1, 16, 21, and 28 to more appropriately define the invention. In particular, amended claims 1, 21, and 28 now specify that the delay matching circuit introduces the second propagation delay to the clock signal without applying the clock signal to a flip-flop. Claim 16 has been amended to correct a typographical error.

Claim Rejection Under 35 U.S.C. § 102

The Examiner rejected claims 1, 3, 13, 21 and 28 under 35 U.S.C. 102(b) as being anticipated by JP Patent No. JP409046189A to Oosera et al. Applicant respectfully traverses this rejection, at least to the extent it may be considered applicable to claims 1, 3, 13, 21, 28, as amended.

In support of the rejection, the Examiner stated that Oosera et al. discloses, in FIG. 1, a clock distribution circuit comprising a clock source 10 to generate a clock signal, and a clock divider 11 including a D flip-flop that introduces a clock-to-Q propagation delay into the divided clock signal. The Examiner further stated that Oosera et al. provides a delay matching circuit 12 that introduces a second propagation delay substantially matching the clock-to-Q propagation delay.

Applicant maintains that the delay circuit 12 described by Oosera et al. does not substantially match the clock-to-Q delay introduced by clock divider 11. Instead, delay circuit 12 appears to be strongly influenced by the reset-to-Q delay in flip-flop 11. As discussed in Applicant's previous response, FIG. 1 of Oosera et al. shows that clock source 10 is coupled to both the clock input (CP) and the set/reset input (CD) of the flip-flop in delay circuit 12. Consequently, the propagation delay produced by the flip-flop in delay circuit 12 would not substantially match the clock-to-Q delay of the flip-flop in clock divider 11.

The reset-to-Q delay is determined by the propagation delay between the reset input and the output of the flip-flop, and is typically different from the clock-to-Q delay in a flip-flop. Oosera et al. assumes that the delays introduced by frequency divider circuit 11 and delay circuit 12 are identical. Although Oosera et al. may intend that the signal delay produced by delay circuit 12 is equal to the delay produced the frequency divider circuit 11, the result may be quite different in operation.

In the Remarks accompanying the final Office Action, the Examiner reiterated the position that Oosera et al. matches a clock-to-Q delay of the flip-flop in the frequency divider circuit 11. In particular, the Examiner stated:

Contrary to the Applicant's analysis, flip-flop 12 does not match a reset-to-Q delay in flip-flop 11, in addition to being coupled to the clock input [CP] the clock source [10] is coupled to the set/reset input [CD], not to match the clock-to-Q delay in the flip-flop driver 11, but rather to provide asserting and disasserting the output of the delay matching circuit 12.

Applicant appreciates the Examiner's efforts to clarify this interpretation of Oosera et al., and understands the Examiner's position. From Applicant's perspective, however, it still appears that the delay circuit 12 of Oosera et al. provides a delay that does not match the clock-to-Q delay of the D flip flop, for reasons further explained below.

Based on Applicant's review, in operation, it appears that delay circuit 12 in the Oosera et al. latches Vcc on the rising edge of clock signal Ai (applied to the CP input) to drive the Q output high, and then resets on the falling edge of clock signal Ai (applied to the CD input) to drive the Q output low. Hence, the propagation delay in the second half cycle, in which the reset drives the Q output low, is strongly influenced by the reset-to-Q (CD-to-Q) delay within the flip-

flop of delay circuit 12. As a result, the delay introduced by delay circuit 12 does not substantially match the clock-to-Q delay of the flip-flop in frequency divider circuit 11.

In view of the above remarks, Applicant continues to believe that Oosera et al. fails to support a prima facie case of anticipation. In the interest of expediting prosecution toward immediate allowance, however, Applicant has made further amendments to claims 1, 21, and 28 make the differences between Oosera et al. and the claimed invention even more clear.

In particular, amended claims 1, 21 and 28 further specify that the delay matching circuit introduces the second propagation delay without applying the clock signal to a flip-flop. Of course, this requirement is directly at odds with the teaching of Oosera et al., in which delay circuit 12 clearly uses a flip-flop to produce delayed clock signal A_o. Therefore, Oosera et al. fails to anticipate the features required by independent claims 1, 21, and 28, as well as dependent claims 3 and 13.

Moreover, with respect to claim 13, Oosera et al. makes no mention of an asynchronous reset feature in delay circuit 12 that mimics operation of an asynchronous reset feature in frequency divider circuit 11. As shown in FIG. 1, CD input of the delay circuit 12 is coupled in common to the clock input of the flip-flop. Therefore, delay circuit 12 cannot be asynchronously reset like frequency divider circuit 11. Instead, CD input is responsive to the clock signal A_i in a synchronous manner.

In view of the differences described above, the Oosera et al. reference fails to anticipate claims 1, 3, 13, 21 and 28, as amended. For at least these reasons, Oosera et al. would not support a prima facie case of anticipation with respect to claims 1, 3, 13, 21 and 28, or any claims dependent on those claims.

Claim Rejection Under 35 U.S.C. § 103

In the Office Action, the Examiner rejected claims 2, 4, 6, 7, 8, 11, 12, 14, 15, 17-19, 22-24, 27, 29, 31, and 33 under 35 U.S.C. 103(a) as being unpatentable over Oosera et al. in view of Chen et al. Applicant maintains that the rejection under section 103 is improper and should be withdrawn. A general discussion of the rejection is set forth below, followed by a more detailed discussion of the rejection as it applies to individual claims.

Oosera et al. clearly fails to disclose the inventions defined by claims 2, 4, 6, 7, 8, 11, 12, 14, 15, 17-19, 22-24, 27, 29, 31, and 33. Chen et al. fails to disclose the features lacking from

Oosera et al.. Moreover, even if such features were described, Chen et al. provides no teaching that would have suggested the desirability modification of the Oosera et al. circuit to arrive at the claimed invention. Hence, Chen et al. lacks both the requisite teachings and the motivation to employ such teachings in the Oosera et al. circuit. The shortcomings of Oosera et al. and Chen et al. will be discussed in more detail below.

In support of the rejections under section 103, the Examiner cited Oosera et al. as disclosing the invention substantially as claimed. The Examiner acknowledged that Oosera et al. fails to disclose various features set forth in the claims, such as a delay matching circuit that includes a multiplexer. However, the Examiner cited Chen et al. as teaching a delay matching circuit including a multiplexer.

On this basis, the Examiner concluded that it would have been obvious to modify the delay matching circuit disclosed by Oosera et al. to include a multiplexer in view of Chen et al. "to facilitate the required delay to enhance system synchronization since such circuit arrangement of the logic circuit for the stated purpose has been a well known practice as evidenced by the teachings of Chen et al."

Applicant strongly disagrees with the Examiner's conclusion of obviousness. The Examiner appears to have relied on Chen et al. for the mere fact that this reference discloses a multiplexer. The Examiner mischaracterized Chen et al. as disclosing a delay matching circuit. Chen et al. does not even disclose a delay matching circuit for matching a propagation delay introduced in a divided clock signal by a flip-flop, however, and makes no mention of delay matching with respect to the circuit shown in FIG. 7 of Chen et al.

Instead, as explained previously by Applicant, the circuit described by Chen et al. in FIG. 7 is very plainly an output buffer circuit. Therefore, it is unclear how or why one of ordinary skill in the art would have even considered modification of the Oosera et al. delay matching circuit in view of the output buffer circuit described by Chen et al. Moreover, it is unclear why the Examiner insists on referring to the output buffer circuit of Chen et al. as a delay matching circuit.

The fact that the output buffer circuit of Chen et al. includes a multiplexer does not make it a delay matching circuit, or amount to any teaching that would have suggested the desirability of using a multiplexer in a delay matching circuit as taught by Oosera et al. Again, Chen et al. provides no teaching remotely pertinent to delay matching. Therefore, it is unclear why one of

ordinary skill in the art would modify a device that already addresses delay matching, i.e., the flip-flop of delay circuit 12 in Oosera et al., with a device that does not having anything to do with delay matching, i.e., the multiplexer shown in FIG. 7 of Chen et al.

Moreover, Chen et al. also lacks any teaching relevant to the additional requirements set forth in Applicant's claims. With respect to claim 7, for example, Applicant finds no teaching in Chen et al. concerning the configuration of the multiplexer of FIG. 7 to have transmission gates that correspond substantially to a slave transmission gate in the flip-flop of a clock divider. Similarly, with respect to claim 14, Applicant is unable to find any mention in Chen et al. of a multiplexer with transmission gates to substantially mimic characteristics of a slave transmission gate of the flip-flop of a clock divider, inputs to substantially mimic characteristics of a master output driver of the flip-flop, or an output to substantially mimic characteristics of an output driver in the flip flop.

Such features are entirely absent from the Chen et al. reference. Indeed, other than pointing to FIG. 7, the Examiner did not identify any support within the Chen et al. reference for such teachings. Therefore, Applicant must ask where the teachings attributed to Chen et al. could have been found.

In reply to arguments previously presented by Applicant in the Amendment filed August 3, 2004, the Examiner stated that Applicants' arguments are moot with respect to claims 2, 4, 6, 12, 14, 15, 17, and 29 in light of the new grounds of rejection based on the combined teachings of Oosera et al. and Chen et al.

In reply to Applicant's arguments concerning claims 4, 6, 12, and 29, in which Applicant stated that "one of ordinary skill in the art would have found no reason to consult Chen et al. for modifications to the Oosera et al. circuit," the Examiner seemed to assert that incorporation of the Chen et al. features would have been obvious because Oosera et al. lacks such features.

Of course, the Examiner's rationale falls far short of a motivation to modify the Oosera et al. circuit in view of Chen et al. In particular, it is insufficient that a reference describe features lacking from Oosera et al. Rather, it is well established that there must be some prior art motivation to make the modifications proposed by the Examiner. Absent such a motivation, the Examiner has clearly failed to establish a prima facie case of obviousness.

The differences between the claimed invention and the Oosera et al. and Chen et al. references are discussed in more detail below with respect to the individual claims.

Claims 2, 4, 6, 12, 14, 18, 19 and 29

With respect to claims 2, 4, 6, 12, and 29, the Examiner recognized that Oosera et al. fails to disclose a delay matching circuit with a multiplexer having transmission gates within the multiplexer to substantially mimic characteristic of a slave transmission gate in a flip-flop, inputs coupled to the multiplexer to substantially mimic characteristics of a master output driver of the flip-flop, and an output coupled to the multiplexer to substantially mimic characteristics of an output driver in the flip flop, as defined by claims 2, 4, 6, 12, 14, 18, 19 and 29.

The Examiner cited Chen et al., however, as teaching such features. On this basis, the Examiner concluded that it would have been obvious to modify Oosera et al. to incorporate the features taught by Chen et al. "to facilitate the required delay to enhance system synchronization since such circuit arrangement of the logic circuit for the stated purpose has been a well known practice as evidenced by the teachings of Chen et al."

The Examiner's conclusion of obviousness is flawed for several reasons. First, Chen et al. does not actually teach the features attributed to it by the Examiner. Second, the Examiner did not identify a motivation to include the features purportedly taught by Chen et al. in the Oosera et al. circuit. Third, if the Oosera et al. circuit were modified to include such features, it is unclear how the Oosera et al. circuit would actually operate. In view of these shortcomings, the rejection of claims 2, 4, 6, 12, 14, 18, 19 and 29 is improper and should be withdrawn.

As discussed above, Chen et al. makes no mention of delay matching in connection with the output buffer circuit of FIG. 7. Chen et al. discloses a multiplexer. However, this multiplexer forms part of an output buffer circuit, not a delay matching circuit for matching a propagation introduced in a divided clock signal by a flip-flop. In the Office Action, the Examiner stated that Chen et al. discloses in "FIG. 7, a delay matching including a multiplexer [and] . . . first and second transmission gates, in which the transmission gates are configured to correspond substantially to a slave transmission gate in the flip-flop." However, it is unclear where the "flip-flop" identified by the Examiner resides within FIG. 7 of Chen et al.

Moreover, the multiplexer disclosed by Chen et al. does include components configured as required by Applicant's claims. For example, none of the components of the multiplexer described by Chen et al. are configured to substantially mimic features of a flip-flop in a clock divider. Indeed, Chen et al. does not even disclose a clock divider or a flip-flop in a clock

divider. Consequently, none of the transmission gates in the Chen et al. circuit are configured to substantially mimic characteristic of a slave transmission gate in a flip-flop of a clock divider.

Therefore, even if the Oosera et al. circuit were modified in view of the Chen et al. teachings, the result would not conform to the requirements of the claimed invention. Applicant has already pointed out that Chen et al. lacks the requisite teachings, in the previous Amendment filed August 3, 2004. Yet, in the final Office Action, the Examiner provided no further clarification concerning this omission. If the Examiner maintains the final rejection in view of Chen et al. Applicant respectfully requests that the Examiner clearly identify the teaching within Chen et al. that would have suggested such features. In the absence of such a teaching, the rejection must be withdrawn.

With respect to the lack of motivation, it is difficult for Applicant to understand how a reference, such as Chen et al., that does not even relate to delay matching, would have motivated one of ordinary skill in the art to modify the Oosera et al. circuit. For example, it is unclear why one of ordinary skill in the art, addressing problems associated with propagation delay matching, would have consulted a reference such as Chen et al., which makes no mention of propagation delay matching, and instead is directed to an output buffer circuit.

If Oosera et al. already provides a solution to the delay matching problem, why would one of ordinary skill in the art consult a reference that does not even mention delay matching? Moreover, why would one of ordinary skill in the art replace delay circuit 12 of Oosera et al. with a multiplexer that serves no delay matching function? The mere presence of a multiplexer or other similar circuitry in Chen et al. does not amount to a teaching that would have suggested modification of a delay matching circuit of Oosera et al. to arrive at the claimed invention.

In the final Office Action, the Examiner provided no further explanation concerning the missing motivation. The vague, universal desire to "facilitate the required delay to enhance system synchronization," as expressed by the Examiner, provides no insight into the precise modifications necessary to arrive at the claimed invention. Without the requisite motivation, the rejection is clearly improper and must be withdrawn.

Finally, even if one of ordinary skill in the art did consult Chen et al., he would have consciously avoided the modification proposed by the Examiner. In particular, it seems that the modification of Oosera et al. to include the features taught by Chen et al. would undermine the operation of the Oosera et al. circuit. Specifically, if the Oosera et al. circuit were somehow

Appl. No. 10/632,651

Amdt. dated 12/9/04

Reply to Office Action of 9/17/04

PATENT

Docket: 020556

modified to include a multiplexer and other components, as taught by Chen et al., it is unclear how the resulting circuit would even be operable.

The Oosera et al. circuit already provides a flip-flop in delay matching circuit 12 for the express purpose of matching the delay of the clock divider. Accordingly, Applicant is confused as to what role the Chen et al. circuitry would actually play in the Oosera et al. circuit. To the extent such circuitry would entirely supplant the Oosera et al. circuit, which already addresses the delay matching issue, then it is unclear how and why one of ordinary skill in the art would have considered such a modification obvious at the time of invention. In the final Office Action, the Examiner provided no further explanation concerning the manner in which Oosera et al. would be modified in view of Chen et al.

In addition to the differences above, there is no mention in Oosera et al. of a delay matching circuit that substantially mimics output drive characteristics of the flip-flop, as in claim 4, nor a multiplexer including a select line coupled to the clock source, as in claim 6. Likewise, Oosera et al. fails to disclose means for mimicking characteristics of slave transmission gates in the flip-flop, means for mimicking characteristics of transistors in a master output driver of the flip-flop, and means for mimic characteristics of an output driver in the flip-flop, as in claim 12. The Examiner did not point to any structure within Chen et al. that would conform to such features, nor explain why modification of Oosera et al. to include them would have been obvious.

Claims 7, 8, 11, 31, and 33

With respect to claims 7, 8, 11, 31 and 33, the Examiner acknowledged that Oosera et al. fails to disclose details of a delay matching circuit including a multiplexer having a first input coupled to drive a first transmission gate, a second input coupled to drive a second transmission gate, a select input coupled to the clock source to selectively enable one of the transmission gates, and an output coupled to the first and second transmission gates, wherein the transmission gates are configured to correspond substantially to a slave transmission gate in the flip-flop, as set forth in claims 7, 8, 11, 31, and 33, or transmission gates are configured to correspond substantially in size to the slave transmission gate in the flip-flop, as recited in claim 8. The Examiner cited the Chen et al. reference for such a teaching, however, and asserted that it would have been obvious to modify the Oosera et al. circuit to include the features taught by Chen et al.

Chen et al. does not provide the teachings attributed to it by the Examiner. Again, Chen et al. makes no mention of a delay matching circuit, nor the various configurations of components within the Chen et al. circuit, to substantially mimic features of a flip-flop in a clock divider. The Examiner broadly asserted that the output buffer circuit in FIG. 7 in Chen et al. contains such features, and pointed to particular transistors, but provided no explanation as to how those transistors meet the structural requirements set forth in the claims.

For example, the multiplexer in FIG. 7 of Chen et al. certainly includes transistors 66, 68, 70, 72, but how did the Examiner determine that they correspond substantially to a slave transmission gate in a flip-flop in a clock divider also required by the claims, e.g., as set forth in claim 7, or correspond substantially in size to such a slave transmission gate, e.g., as set forth in claim 8? Without such an explanation, the Examiner's analysis overlooks these clear requirements of Applicant's claims. Consequently, the rejection is improper and must be withdrawn.

In view of these basic deficiencies, Oosera et al. and Chen et al. clearly would not support a prima facie case of unpatentability. Moreover, as expressed above, Applicant questions why one of ordinary skill in the art would have looked to the teachings of Chen et al., which appear to bear no relationship to the delay matching problem, much less provide a solution to that problem.

Claims 15, 17, 22-24 and 27

With respect to claims 15, 17, 22-24 and 27, the Examiner recognized that Oosera et al. fails to disclose various details of a delay matching circuit, but again cited Chen et al. for such a teaching. For substantially the same reasons discussed above, Applicant respectfully submits that Chen et al., which contemplates no delay matching circuit, provides no teaching that would have suggested the requisite modifications to the Oosera et al. circuit to arrive at the invention of claims 22-24 and 27. Nor would one of ordinary skill in the art have even looked to Chen et al. in contemplation of the delay matching problems addressed by Oosera et al.

Appl. No. 10/632,651

Amdt. dated 12/9/04

Reply to Office Action of 9/17/04

PATENT

Docket: 020556

CONCLUSION

All claims in this application are in condition for allowance. Applicant respectfully requests reconsideration and prompt allowance of all pending claims. Please charge any additional fees or credit any overpayment to deposit account number 17-0026. The Examiner is invited to telephone the below-signed attorney to discuss this application.

Respectfully submitted,

Dated: 12/9/04

By: 

George C. Pappas, Reg. No. 35,065
858-651-1306

QUALCOMM Incorporated
Attn: Patent Department
5775 Morehouse Drive
San Diego, California 92121-1714
Telephone: (858) 658-5787
Facsimile: (858) 658-2502